Low Noise High Efficiency 3.75 µm and 2.8 µm Global Shutter CMOS Pixel Arrays

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Introduction

The general trend of reducing the pixel size while maintaining the image sensor performance is directly applied to the global shutter (GS) pixel development at Aptina as illustrated in Figure 1. To compete successfully with previous generation devices, smaller pixels require higher sensitivity or quantum efficiency (QE), smaller noise floor, and larger arrays size.

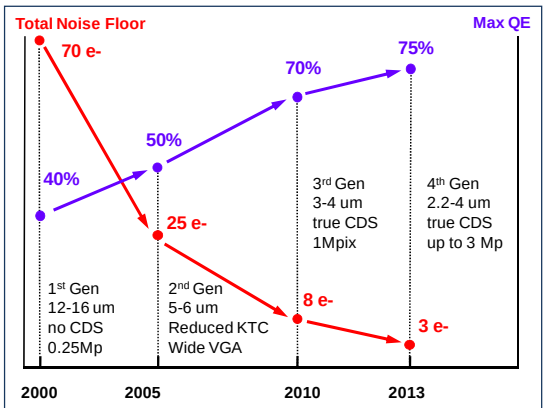

Figure 1. Global shutter pixel development

Our history of GS pixel development started at Photobit Corporation in the late 90s by creating the 1st generation of GS sensors for machine vision applications with pixel size in the range of 12µm to 16µm, sensor format up to 512x512 pixels, and frame rate up to 5000FPS. Sensors achieved quantum efficiency (QE) of 40% and noise floor of 70e [1]. A 2nd generation of Global shutter devices was developed in 2005 by the Micron Imaging group [2]. Pixel size was reduced to 6.0µm, QE was increased to 50%, and noise floor was reduced to ~25e by using soft reset of the floating diffusion. High dynamic range feature was also added to design of the sensor. The range of applications was significantly extended as these devices are successfully utilized now in automotive, surveillance, and gaming applications. True correlated double sampling (CDS) technique was introduced in the 3rd generation of Aptina GS pixels to significantly reduce the sensor noise floor. Additionally, the pixel shared architectures allowed further shrinking of the pixel size. QE was increased to 70%. Progressing from a floating diffusion (FD) as a pixel memory to a dedicated in-pixel pinned diode charge storage allowed significant reduction of the readout noise (up to 2.4e) and total noise floor (8e). The 3rd generation pixel and sensors were first presented in 2011 [3]. In this paper we present the progress in pixel performance improvement that was made since then and also present development of next generation of GS pixel design allowing for the further pixel shrink and performance improvement.

3rd generation 3.75µm GS pixel

The 3rd generation of GS pixel 4T effective in a 2-way common element pixel architecture (CEPA) and associated potential diagram of operation are illustrated in Figure 2. The storage node (SN) consists of a pinned storage buried diode that receives charge from the photodiode via the first transfer gate. Photon generated charge accumulated in the PD is globally transferred via the first transfer gate to the pixel storage node. Charge is read out row by row by transferring it from the pixel SN to the FD via the second transfer gate to implement the correlated double sampling (CDS) operation. Although implementing the true CDS operation, this architecture nevertheless suffers from a relatively high dark current and limited full-well

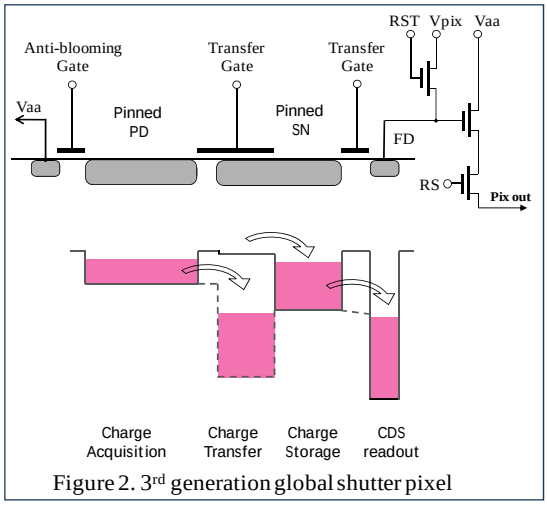

Figure 2. 3rd generation global shutter pixel

capacity due to the non-optimal utilization of Si area and partition of the voltage budget between PD, SN, and FD. With practical layout limitations on the actual pixel design, keeping the balance between capacities of photodiode and the storage node requires a pretty high pinned potential of the diode in the storage node, which results in higher dark current. This also limits the potential swing on the FD, thus resulting in tradeoff between full-well capacity of the pixel and FD conversion gain / readout noise. The careful engineering of transfer gate and the pinned buried diode storage has reduced the overall dark current to an acceptable level that was measured lower in comparison to the 2nd generation pixel (see Table 1 Gen 2 vs. Gen 3 storage dark current).

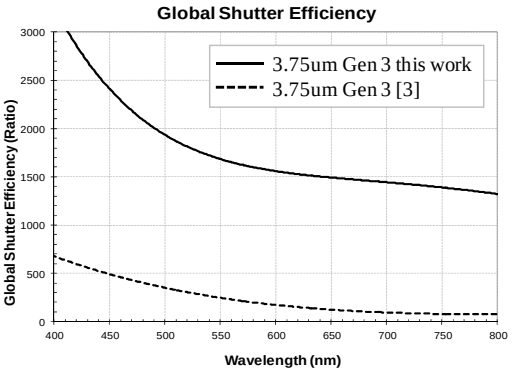

Figure 3. Global shutter efficiency for 3rd gen 3.75um pixel

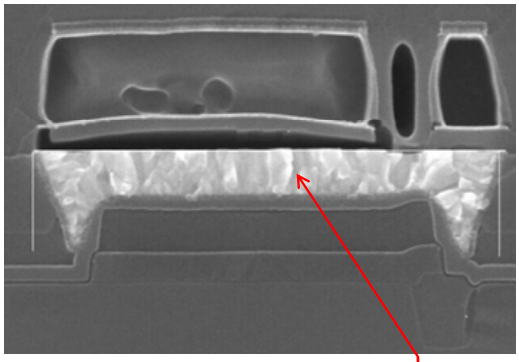
Figure 4. Optical isolation of SN with tungsten buried light shield

Significant progress has also been made in relation to the global shutter efficiency (GSE) of the 3rd generation 3.75µm GS pixel. Improvement of electrical and optical isolation of the pixel storage node resulted in a GSE increase above 1500:1 in comparison to the previously reported value of 310:1 [3], as well as in a more uniform GSE performance across a wide wavelength spectrum. Figure 3 presents GSE as a function of wavelengths for 3.75µm pixel. GSE ranges above 2000:1 at short wavelengths and drops below 1500:1 at the near-IR wavelengths. It is worth mentioning that the GSE performance is better at the shorter wavelengths partially because the poly-silicon gates shield the storage node. The characterization of the GSE performance vs. specific wavelength band guarantees the sensor performance for different applications starting with the blue and red wavelengths commonly used for scanning applications and finishing with the visual and near-IR wavelength ranges that are important for the automotive, gaming, and other emerging applications. One of the optical isolation techniques used in these sensors is a tungsten buried light shield (WBLS) wrapped around the storage gate below the metal 1 to shield the storage node from incident light (see Figure 4). Engineering of the PD and storage implants additionally improved the GSE by further shielding the pixel storage area from parasitic charge collection.

Figure 5 shows a comparison of SNR between the 3rd generation 3.75µm GS pixel with the previous generation 6.0µm GS pixel. In spite of the much smaller pixel size, the 3.75µm pixel outperforms the 6.0µm pixel at small exposures, and only slightly yields to 6.0µm pixel performance at high exposures where SNR values are pretty high. With increased array size, the overall image quality of the 3rd generation GS sensors are better than that of the 2nd generation GS sensor, which allowed further extension of applications, including both portable and handheld scanning devices. Figure 6 presents images taken with a 1Mpix sensor with the 3rd gen 3.75µm GS pixel compared to its counterpart with a rolling shutter pixel [4]. Image quality of the GS sensor approaches the quality of the rolling shutter sensor.

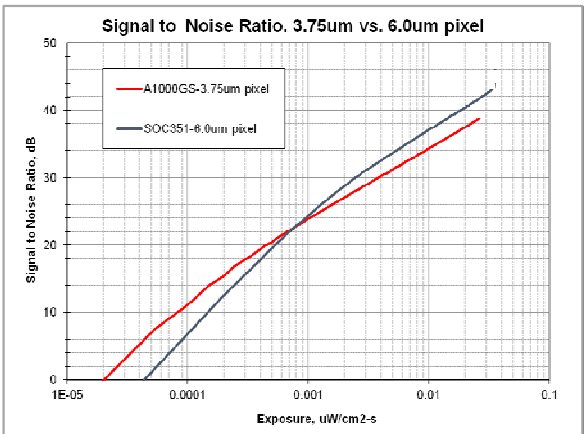

Figure 5. Temporal SNR as a function of exposure for 3.75 µm 3rd gen and 6.0µm 2nd gen GS pixels

a. b.

Figure 6. Image of the rotating fan taken with GS and RS sensors:
a. 1Mpix sensor, 3.75µm rolling shutter pixel b. 1Mpix sensor, 3.75µm global shutter pixel

4th generation GS pixel

The 4th generation of GS pixel is using completely pinned low dark current diode as a storage node (SN), and employs Aptina's patented charge pumping transfer method and a special design of the transfer pump gate (PG). The charge pumping transfer method can be applied to both the transferring charge from PD to SN for storage and to transferring charge from SN to FD for readout. Figure 7 illustrates an example of the PG located between PD and SN. The PG is engineered to have a lower potential on one side (next to PD) to prevent charge from spilling back to PD during transfer operation. An additional small size diode with low pinned potential is placed between PG and SN. This additional barrier diode serves as a virtual barrier (VB) between SN and PG and prevents charge from spilling back to PG during the transfer operation. To reduce the area overhead, the size of PG and corresponding charge handling capacity is chosen to be relatively small. A charge transfer procedure includes several cycles of clocking PG while a small portion of charge is transferred during each cycle until the entire charge acquired on PD during the integration time is transferred to the SN (see Figure 7).

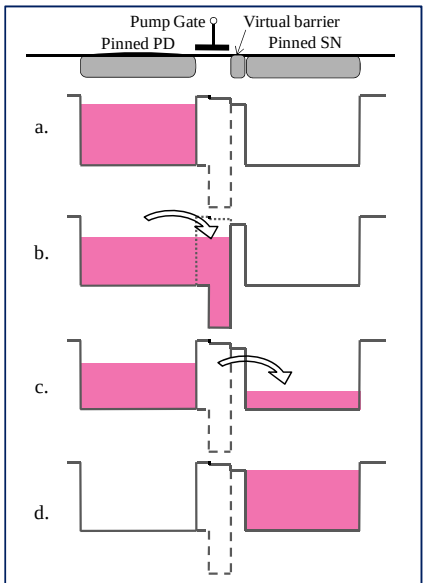

Figure 7. Transferring charge with pump gate.
a.- before transferring, b.– first transfer cycle,
c.– after first transfer cycle, d.- after N transfers

Note, that the pinned potential of the 1st node where the charge is transferred from (e.g. the pinned PD in Figure 7) could be very close to the potential of the 2nd node where the charge is transferred to (in this case, the pinned SN), thus preserving the voltage budget from dividing between the nodes. Extending the pump gate approach to the transfer of charge between the SN and FD enables a higher conversion gain of the FD without reducing FD charge handling capacity and correspondingly lower readout noise. In summary, the charge pumping approach allows a very effective GS pixel layout with high utilization of Si area and better partitioning of voltage budget between PD, SN, and FD. It benefits major characteristics of GS pixel: pixel capacity, dark current, and readout noise – and opens the road for further pixel shrinks. The 4th generation GS pixel architecture was implemented into 3.75µm and 2.8µm test pixel arrays using 0.13µm manufacturing process. Comparing to the 3rd generation pixel, we have achieved a significant reduction of dark current (an order of magnitude), 2x increase of the pixel well capacity, and reduction of total noise in the dark conditions to 2e – 3e.

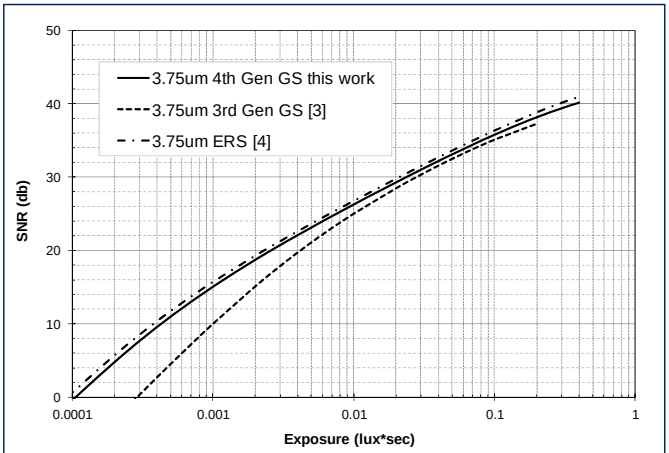

Figure 8. Total SN ratio as a function of exposure for 3.75 µm GS and RS pixels

Figure 8 presents total SN ratio as a function of exposure. Performance of the 4th generation 3.75µm GS pixel is compared with the 3rd generation 3.75µm GS pixel and with the 3.75µm rolling shutter pixel [4]. As can be seen from the plot our 4th generation GS pixel outperforms the 3rd generation GS pixel in low light sensitivity and SNR at high exposures due to improvement in dark current, readout noise, and full well capacity. A summary of pixel characteristics is presented in Table 1.

Work is also in progress to further improve GSE by employing more optical and electrical isolation of the storage node. Introduction of a light guide resulted in more than the two times better GSE as was demonstrated with the latest improved designs. Additionally, the light guide allows for a wider acceptance angle of light and reduces the effective optical stack height of these front side illuminated (FSI) pixels.

Table 1

	Unit	Gen2 [2]	Gen3 [3]	Gen3	Gen4		Note
Pixel Pitch	um	6	3.75	3.75	3.75	2.8	
True CDS		No	Yes	Yes	Yes	Yes	
Max Quantum Efficiency	%	58	70	70	75	70	mono
Linear Full-well	Ke-	17.5	7.5	7.5	> 15	> 12	
Pixel Response Non-uniformity	%	0.7	0.8	0.8	0.6	0.6	50% signal
Pixel Total Noise Floor	e-	25	8	8	3	3	25C Tj
Storage Dark Current	e-/sec	3000	2000	2000	90	60	60C Tj
Global Shutter Efficiency	ratio	1700	310	2000	3000	2200	average

Conclusion

We have successfully demonstrated a 4th generation GS pixel architecture that utilizes a pumping charge transfer method. This architecture significantly benefits pixel performance, opens the road for further pixel shrinks, and promises extension of the applications range. The 4th generation architecture is implemented in 3.75µm pixel and 2.8µm pixel, which is, according to our knowledge, the smallest GS pixel with true CDS published to date in CMOS. We have also demonstrated significant improvement of the 3rd generation GS pixel with 3.75µm pixel size in shutter efficiency, dark current, and noise floor compared to first introduction of this pixel to the market.

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